What is claimed is:

1. An apparatus to tune a tunable Gm-C circuit, the apparatus comprising:

a master Gm-C circuit comprising a tunable element, wherein the master Gm-C circuit is configured to provide a waveform that is dependent on a tuning signal that is applied to the tunable element;

a precision signal generator to provide a precision signal;

a sampler having a first input coupled to the waveform from the master Gm-C circuit, a second input coupled to the precision signal, and an output to provide a tuning error signal; and

a tuning control stage having an input coupled to the output of the sampler and having an output to provide the tuning signal to the master Gm-C circuit and to the tunable Gm-C circuit.

2. An apparatus as defined in Claim 1, wherein the sampler provides a tuning error signal that is dependent a relationship between the precision signal generator and waveform provided by the master Gm-C circuit.

3. An apparatus as defined in Claim 2, wherein the tuning error signal assumes a first value in response to a tuning error in a first direction and assumes a second value in response to a tuning error in a second direction.

4. An apparatus as defined in Claim 3, wherein the first circuit comprises a comparator and the second circuit comprises a sampler.

5. An apparatus to tune a Gm-C circuit, the apparatus comprising:

a time-constant circuit comprising a master controllable element matched to a slave controllable element in the Gm-C circuit;

a comparator coupled to the time-constant circuit;

a sampler coupled to the comparator, the counter to generate a tuning error signal; and

a tuning control stage coupled to the sampler to provide a corrected tuning voltage to the master controllable element in the time-constant circuit and to the slave controllable element in the Gm-C circuit.

6. An apparatus as defined in Claim 5, wherein the comparator comprises a first input coupled to a reference voltage and a second input coupled to the time constant circuit, wherein the comparator is operative to provide a comparator output signal determined by the relationship between reference voltage and a ramping voltage from the time-constant circuit.

7. An apparatus as defined in Claim 6, wherein the comparator is configured to provide a comparator output signal to the sampler so that the sampler generates a

tuning error signal in response to a transition in the comparator output signal.

8. An apparatus as defined in Claim 5, wherein the tuning control stage is operative in response to the tuning error signal so that the tuning control stage effects correction of the tuning voltages in a first direction in response to a first value of the tuning error signal and effects correction of the tuning voltage in a second direction in response to a second value of the tuning error signal.

9. An apparatus as defined in Claim 8, wherein the comparator comprises a first input coupled to a reference voltage and a second input coupled to the time constant circuit, wherein the comparator is operative to provide an output signal determined by the relationship between reference voltage and a ramping voltage from the time-constant circuit.

10. An apparatus as defined in Claim 9, wherein the comparator is configured to provide an output signal to the sampler so that the sampler generates a tuning error signal in response to a transition in the comparator output signal.

11. An apparatus as defined in Claim 8, wherein the tuning control stage is configured to provide, during the course of a tuning process, a sequence of digital tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

12. An apparatus as defined in Claim 11, wherein the tuning control stage is configured to provide a predetermined initial digital tuning signal at inception of a tuning process and to provide subsequent sequential digital tuning signals in response to operation of the time-constant circuit.

13. A method comprising:

effecting a time period that is related to a master controllable tuning element;

enabling a counter to operate during the time period;

sampling an output of the counter upon expiration of the time period;

coupling an output of the counter, upon expiration of the time period, to a tuning control stage;

in the tuning control stage, providing a tuning signal in response to the output of the counter upon expiration of the time period; and

coupling the tuning signal to a slave controllable tuning element.

14. A method as defined in Claim 13, wherein effecting a time period comprises:

causing a time-varying signal to be applied from a time-constant circuit to a first input of a comparator, wherein the comparator comprises a second input to which there is applied a reference signal.

15. A method as defined in Claim 14, wherein the time-constant circuit comprises a master controllable component that is controlled by the tuning voltage.

16. A method as defined in Claim 15, further comprising:

applying a corrected tuning voltage to the time-constant circuit so as to control the master controllable component in a manner that causes a value of the master controllable component to approach a predetermined value.

17. A method as defined in Claim 16, further comprising:

applying the corrected tuning voltage to a slave controllable component.

18. A method as defined in Claim 17, wherein the master controllable component and the slave controllable component are capacitances.

19. A method as defined in Claim 17, wherein the master controllable component and the slave controllable component are transconductances.

20. A method as defined in Claim 17, wherein the tuning control stage provides a predetermined initial digital tuning signal at inception of a tuning process and provides sequential tuning signals in response to a tuning error signal form the counter and wherein subsequent tuning signals incorporate a correction, the polarity of a correction being determined by the tuning error signal and the magnitude of a correction being determined by an immediately preceding correction..

21. A method as defined in Claim 13, further comprising:

in the tuning control stage, providing an initial digital tuning signal upon inception of a tuning process.

22. A method as defined in Claim 21, further comprising:

providing, in the tuning control stage during the course of a tuning process, a sequence of digital tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal within a predetermined precision.

23. A method as defined in Claim 22, further comprising:

driving the counter with a clock signal that has a clock period that is related to an ideal tuning voltage.

24. A method as defined in Claim 23, wherein sampling the counter output results in a binary sampling signal that is used to determine the direction of correction imparted to a then-existing digital tuning signal.

25. A method as defined in Claim 23, further comprising:

charging the master controllable tuning element to a predetermined reference voltage;

determining the value of an output of the counter at a sampling instant that corresponds to the expiration of the time period; and

effecting a correction in the tuning voltage, wherein the direction of the correction is determined by a sampled value of the counter output and the magnitude of the correction is a function of an immediately preceding correction.

26. A method as defined in Claim 25, wherein the tuning signal is a digital signal and wherein completion of

a tuning process is determined by detection of successive values of a least significant bit of the digital tuning signal.

27. An article comprising a machine-readable storage medium on which there are stored instructions that, if executed, enable the system to:

effect a time-period that depends on a master controllable tuning element;

enable a clock to operate during the time period, the clock having predetermined a clock period;

sample an output of the clock upon expiration of the time period;

derive a binary signal from the sampled clock output; and

develop a digital tuning signal in response to the sampled clock output, the digital tuning signal to be coupled to the master controllable tuning element and to the slave controllable tuning element.

28. An article as defined in Claim 27, further comprising instructions that, if executed, enable the system to:

provide an initial digital tuning signal upon inception of a tuning process.

29. An article as defined in Claim 28, wherein the initial digital tuning signal corresponds to approximately a midpoint of an applicable tuning range.

30. An article as defined in Claim 28, further comprising instructions that, if executed, enable the system to provide, in the course of the tuning process, a sequence of digital tuning signals, wherein the sequence of digital tuning signal converges to a final digital tuning signal that approximates an ideal digital tuning signal within a predetermined precision.

31. A tuning apparatus comprising:

a waveform generator to provide a time-varying waveform, the waveform generator comprising a master controllable tuning element;

a clock generator to provide a precision clock signal;

means responsive to the time-varying waveform for sampling the precision clock signal; and

a tuning control stage coupled to the means for sampling to generate a corrected tuning signal in response to an output of the means for sampling, the corrected tuning signal to be provided to the master controllable tuning element and to a slave controllable tuning element.

32. A tuning apparatus as defined in Claim 31, wherein the master controllable tuning element is matched to the slave controllable tuning element.

33. A tuning apparatus as defined in Claim 31, wherein the sampling means comprises:

a first circuit to provide a binary output signal that has a value determined by the time-varying waveform; and

a second circuit coupled to the first circuit and to the clock generator, the second circuit to provide a tuning error signal.

34. A tuning apparatus as defined in Claim 33, wherein the tuning error signal assumes a first value in response to a tuning error in a first direction and assumes a second value in response to a tuning error in a second direction.

35. A tuning apparatus as defined in Claim 33, wherein the first circuit comprises a comparator and the second circuit comprises a sampler.

36. A tuning apparatus as defined in Claim 35, wherein the comparator comprises a first input coupled to a reference voltage and a second input coupled to the waveform generator circuit, wherein the comparator is operative to provide a comparator output signal determined by the relationship between the reference voltage and the time varying waveform.

37. A tuning apparatus as defined in Claim 33, wherein the tuning control stage is operative in response to the tuning error signal so that the tuning control stage effects correction of the tuning signal in a first

direction in response to a first value of the tuning error signal and effects correction of the tuning signal in a second direction in response to a second value of the tuning error signal.

38. A tuning apparatus as defined in Claim 37, wherein the tuning control stage is configured to provide, during the course of a tuning process, a sequence of digital tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

39. A tuning apparatus as defined in Claim 38, wherein the correction stage is configured to provide a predetermined initial digital tuning signal at inception of a tuning process and to provide subsequent sequential digital tuning signals in response to operation of the waveform generator.

40. A tuning apparatus as defined in Claim 39, wherein the first circuit comprises a comparator and the second circuit comprises a sampler.

41. A tuning apparatus as defined in Claim 40, wherein the comparator comprises a first input coupled to a reference voltage and a second input coupled to the

waveform generator circuit, wherein the comparator is operative to provide a comparator output signal determined by the relationship between reference voltage and the time varying waveform.

42. A tuning apparatus as defined in Claim 39, wherein the tuning control stage is configured to effect successive corrections in the digital tuning signal, wherein the direction of a correction is responsive to a value of an output of the means for sampling and the magnitude of a correction is a function of an immediately preceding correction.

43. A system comprising:

a low-noise amplifier (LNA) to receive a modulated carrier;

a mixer coupled to the LNA;

a demodulator coupled to the mixer;

a tunable baseband filter coupled to the demodulator;

an apparatus to tune the filter, the apparatus comprising:

a waveform generator to provide a time-varying waveform, the waveform generator comprising a master controllable tuning element;

a clock generator to provide a precision clock signal;

a sampling circuit responsive to the time-varying waveform to sample the precision clock signal; and

a tuning control stage coupled to the sampling circuit to generate a corrected tuning signal in response to an output of the sampling circuit, the corrected tuning signal to be provided to the master controllable tuning element and to a slave controllable tuning element in the filter.

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44. A tuning apparatus as defined in Claim 43, wherein the master controllable tuning element is matched to the slave controllable tuning element.

45. A tuning apparatus as defined in Claim 43, wherein the sampling circuit comprises:

a first circuit to provide a binary output signal that has a value determined by the relationship of the time-varying waveform to the clock generator; and

a second circuit coupled to the first circuit and to the clock generator, the second circuit to provide a tuning error signal.

46. A tuning apparatus as defined in Claim 45, wherein the tuning control stage is operative in response to the tuning error signal so that the tuning correction stage effects control of the tuning signal in a first direction in response to a first value of the tuning error signal and effects correction of the tuning signal in a second direction in response to a second value of the tuner error signal.

47. A tuning apparatus as defined in Claim 46, wherein the tuning control stage is configured to provide, during the course of a tuning process, a sequence of digital tuning signals, wherein the sequence of digital

tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

48. A tuning apparatus as defined in Claim 47, wherein the tuning stage is configured to provide a predetermined initial digital tuning signal at inception of a tuning process and to provide subsequent sequential digital tuning signals in response to operation of the waveform generator.